

1 **ABSTRACT**

2 A circuit and method for synchronized clocking of components such as  
3 registers. Registers are clocked by individual component clock signals having the  
4 same frequency but potentially different phases due to differing propagation  
5 delays. Separate component clock signals are received by registers are brought  
6 into phase by evaluating the phases of the component clock signals at the registers,  
7 and synchronizing the component clock signal of each register to that of the  
8 previous register in a sequence.  
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